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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,651	01/10/2005	Yin Tat Ma	UC1.PAU.05US	5137

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	PAPER NUMBER
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/501,651	MA ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5,6,8,9,11-15,17-23 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 18-20* is/are allowed.

6)☒ Claim(s) *1,5,8,9,12-14,21-23,25 and 26* is/are rejected.

7)☒ Claim(s) *6, 15, 17, 27, 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 5, 9, 12-14, 21-22, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., Patent No. 5,774,318, in view of Davis, Patent No. 6,529,059.

With respect to claim 1, McClure et al. teaches an electrostatic discharge protection circuit [Fig. 2] coupled to ground [Fig. 2, 104] comprising: an input [Fig. 2, Vcc 102]; a diode string [Fig. 2, 100] coupled to the input; a transistor switch [Fig. 2, Q3, 106] having its gate coupled to the diode string, the transistor switch coupling the input to ground in parallel to the diode string; and a reverse diode [Fig. 2, 116] coupling ground to the input as disclosed in Col. 3, lines 19-25 and lines 44-48. However, McClure does not disclose a capacitive element and voltage overload protection for RF power amplifiers.

Davis teaches an ESD protection for an integrated circuit. Davis teaches a capacitive element [Fig. 3, D1, D2] in series with the transistor switch [Fig. 3, 16c] to reduce the capacitance contributed by the transistor switch, thereby reducing signal distortion [Col. 4, lines 54-57; Col. 4, line 65–Col. 5, line3]; whereby voltage overload protection for RF power amplifiers [Col. 2, lines 56-59]

is provided for the conditions of output impedance mismatch, RF overdrive, and modulated input signal [Col. 1, lines 57-65].

Both teachings are analogous electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Davis, which teaches a capacitive elements which reduces the capacitance and a voltage overload protection for RF power amplifier, with the ESD protection circuit of McClure, for the benefit of reducing the loss of signal provided by integrated circuit by reducing the capacitance on the transistor.

With respect to claim 5, Davis teaches that the transistor comprises a single bipolar transistor [Fig. 3, 16C] and the capacitive element comprises a diode [Fig. 3, D1, D2], but does not disclose that the switching transistor comprises a Darlington pair. McClure teaches that a Darlington pair [Fig. 3, Q4, Q5, 106] is preferred over a single transistor [Fig. 2, Q3, 106, Col. 5, lines 55-65]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the switching transistor [Fig. 4, Q1] taught by Weiss with the switching transistor [Fig. 3, Q4, Q5, 106] to have a Darlington pair and a diode in series, because the Darlington pair offers a higher gain and thus a faster turn-on time, as well as a higher collector impedance which results in a lower leakage current.

With respect to claim 9, Davis teaches that the electrostatic discharge protection circuit is integrally coupled to the input/output signal terminal of an RF integrated circuit [Col. 2, lines 51-59].

With respect to claim 12, McClure teaches a method for providing electrostatic discharge protection for an input/output signal terminal of an integrated circuit comprising sinking a first type of ESD event to ground [Fig. 1, GND 104] from an input/output signal terminal [Fig. 1, Vcc, 102] through a diode string [Fig. 1, 100] coupled to the input/output signal terminal by triggering a transistor switch [Fig. 1, Q3, 106] having its gate coupled to the diode string, the transistor switch coupling the input/output signal terminal to ground in parallel to the diode string; and sinking a second type of ESD event through a reverse diode [Fig. 1, 116] coupling ground to the input/output signal terminal [Col. 3, lines 19-25, lines 38-41, lines 44-48, Col. 5, lines 7-16, Col. 6, lines 18-21]. However, McClure does not disclose a capacitive element.

Davis teaches an ESD protection for an integrated circuit. Davis teaches coupling the input/output signal terminal [Fig. 3, 14c] to ground during ESD protection by means of a capacitive element [Fig. 3, D1, D2] in series with the transistor switch [Fig. 3, 16c] to reduce the capacitance contributed from the transistor switch, thereby reducing signal distortion [Col. 4, lines 65–Col. 5, lines 3].

With respect to claim 13, McClure teaches that the first type of ESD event is a positive voltage surge applied to the input [Col. 3, lines 19-25, lines 38-41],

and the second type of ESD event is a negative voltage surge applied to the input [Col. 5, lines 7-16, Col. 6, lines 18-21].

With respect to claim 14, McClure teaches that triggering the transistor switch comprises triggering a Darlington pair [Fig. 3, Q4, Q5, 106].

With respect to claim 21, McClure teaches that the diode string [Fig. 2, 100] is comprised of a plurality of BC junction diodes [Fig. 3, 115].

With respect to claim 22, the limitation is the polar opposite of claim 21, and is an art recognized equivalent configuration.

With respect to claim 25, McClure teaches an ESD protected bonding pad comprising a first pad [Fig. 2, Vcc, 102]; a diode string [Fig. 2, 100] coupled to the first pad; a transistor switch [Fig. 2, Q3, 103] having its gate coupled to the diode string, the transistor switch coupling the first pad to ground in parallel to the diode string; and a reverse diode [Fig. 2, 116] coupling ground to the first pad as disclosed in Col. 3, lines 19-25 and lines 44-48. However, McClure does not disclose a capacitive element in series with the transistor switch.

Davis teaches an ESD protection for an integrated circuit. Davis teaches a capacitive element [Fig. 3, D1, D2] in series with the transistor switch [Fig. 3, 16c] to reduce the capacitance contributed by the transistor switch, thereby reducing signal distortion [Col. 4, lines 54-57; Col. 4, line 65–Col. 5, line3].

Both teachings are analogous electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Davis, which teaches a

capacitive elements which reduces the capacitance and a voltage overload protection for RF power amplifier, with the ESD protection circuit of McClure, for the benefit of reducing the loss of signal provided by integrated circuit by reducing the capacitance on the transistor.

With respect to claim 26, McClure teaches an ESD protected integrated circuit input comprising an integrated circuit input [Fig. 2, Vcc, 102]; a diode string [Fig. 2, 100] coupled to the integrated circuit input; a transistor switch [Fig. 2, Q3, 106] having its gate coupled to the diode string, the transistor switch coupling the integrated circuit input to ground in parallel to the diode string; and a reverse diode [Fig. 2, 116] coupling ground to the integrated circuit input as disclosed in Col. 3, lines 19-25 and lines 44-48.

Davis teaches an ESD protection for an integrated circuit. Davis teaches a capacitive element [Fig. 3, D1, D2] in series with the transistor switch [Fig. 3, 16c] to reduce the capacitance contributed by the transistor switch, thereby reducing signal distortion [Col. 4, lines 54-57; Col. 4, line 65–Col. 5, line3].

2. Claims 8 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., Patent No. 5,774,318, in view of Davis, Patent No. 6,529,059, and further in view of Brennan et al., Publication No. US2002/0130392. McClure teaches an ESD protection circuit coupled to ground that comprises a diode string, transistor switch and reverse diode, but does not disclose that the diode string, transistor switch and reverse diode is fabricated in GaAs, InP, SiGe, or other compound semiconductor.

Brennan teaches an ESD protection circuit [Fig. 20] that uses SiGe transistors, and SiGe diodes [Page 3, paragraph 35]. Both teachings are related by being electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brennan, which teaches transistors and diodes fabricated in SiGe, with the ESD protection circuit of McClure for the benefit of using fabricated ESD resistant SiGe devices in either high-frequency ESD protection circuits or for high-frequency driver/receiver (D/R) circuits.

With respect to claim 23, McClure teaches that the diode string is comprised of a plurality of isolated implanted base collector diodes [Fig. 3, 100, 115], but does not disclose that the base collector diodes are fabricated in compound semiconductor technology, including GaAs, InP or other compound semiconductor. Brennan teaches an ESD protection circuit [Fig. 20] that uses SiGe transistors, and SiGe diodes [Page 3, paragraph 35].

Allowable Subject Matter

3. Claims 6, 15, 17, 27, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 6: The prior art teaches that the transistor switch comprises a Darlington pair, but further does not disclose a series diode and a series resistor combined in any order and coupled between the gate of the transistor switch and

the diode string on one hand and ground on the other hand. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 15: The prior art does not disclose that the Darlington pair coupling the first type of ESD event through the diode string to a series diode and resistor to ground to prevent the ESD protection circuit from turning on during low to moderate RF power operation, therefore minimizing leaking current and improving linearity. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 17: The prior art does not disclose that coupling the input to ground during ESD protection comprises coupling the input to ground by means of a diode in series with a Darlington pair to reduce the capacitance contributed from the Darlington pair, thereby reducing signal distortion. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 27: The prior art does not disclose that the transistor switch and diode string each have a chip-layout size and where the chip-layout size of the transistor switch and diode string when used in combination is smaller than the chip-layout size of a diode string when used alone, which used-alone diode

string provides substantially the same ESD protection as the transistor switch and diode string in combination as characterized by the maximum clamping voltage of the electrostatic discharge protection circuit. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

4. Claims 11 and 18-20 are allowed.

The following is an examiner's statement of reasons for indicating allowance of claim 11: The prior art does not disclose a Darlington pair having its gate coupled to the diode string, the Darlington pair coupling the input/output signal terminal to ground in parallel to the diode string; a series diode; a series resistor; a diode in series with the Darlington pair to reduce the capacitance contributed by the Darlington pair, thereby reducing signal distortion. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 18: The prior art does not disclose coupling the first type of ESD event through the diode string to the gate of the Darlington pair couples the first type of ESD event through the diode string to a series diode and resistor to ground to prevent the ESD protection circuit from turning on during low to moderate RF power operation, therefore minimizing leaking current and improving linearity, while also coupling the input/output signal terminal to ground during the ESD protection by means of a diode in series with the Darlington pair

to reduce the capacitance contributed to the diode string from the Darlington pair thereby reducing signal distortion. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

Response to Arguments

5. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Applicant comments on page 12 of the remarks that McClure does not disclose the amended claim 1 regarding a capacitive element in series with transistor, and reducing signal distortion.

A new reference by Davis [Patent No. 6,529,059] teaches this limitation. Davis teaches an ESD protection circuit for an integrated circuit, in which the circuit comprises a capacitive element [Fig. 3, D1, D2] in series with the transistor switch [Fig. 3, 16c] to reduce the capacitance contributed by the transistor switch, thereby reducing signal distortion [Col. 4, lines 54-57; Col. 4, line 65–Col. 5, line3]; whereby voltage overload protection for RF power amplifiers [Col. 2, lines 56-59] is provided for the conditions of output impedance mismatch, RF overdrive, and modulated input signal [Col. 1, lines 57-65]. [See above rejection for claim 1].

Applicant comments on page 13 of the remarks that McClure does not disclose the amended claim 12 regarding reducing signal distortion [See rejection for claim 12].

Applicant comments on page 14 of the remarks that McClure does not disclose the amended claims 25 and 26 regarding a capacitive element in series with the transistor switch to reduce the capacitance contributed by the transistor switch, thereby reducing signal distortion. [See the above rejections for claims 25 and 26; also see the above response to this limitation].

Applicant comments on pages 15-17 of the remarks regarding the prior art references by Weiss and Ring. These references re not used to reject any of the claims. A new reference by Davis is used with McClure to read on the amended claim language.

Applicant comments on pages18-20 the remarks regarding claims 6 and 15. The arguments are not moot, because these claims have allowable subject matter.

Applicant comments on page 20 regarding claims 8 and 23. However, a new reference by Davis is introduced to reject the amended claim 1. The arguments regarding claims 8 and 23 are not moot.

Applicant comments on page 20 of the remarks regarding claims 9 and 10. A new reference by Davis is used to reject the amended claim 1. The arguments regarding Johnson reference are moot.

Applicant comments on pages 1-33 of the remarks regarding claims 11 and 18-20. These claims are allowable, since the arguments and the amendments to claims 11 and 18 have overcome the rejections.

Applicant comments on pages 33-34 of the remarks regarding claims 27 and 30. Theses claims have allowable subject matter, so the arguments regarding these claims are moot.

Based on examiner's best understanding, it is believed that the prior art references by McClure and Davis read on the amended claim language of independent claims 1, 12, 25 and 26. Accordingly,

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DHP
01/24/2007

Stephen W Jackson
1-25-07

STEPHEN W. JACKSON
PRIMARY EXAMINER